REMARKS/ARGUMENTS

I. Status of the Claims

Prior to entry of this amendment, claims 1-3, 8-10 and 13-17 were pending for examination. An office action mailed June 14, 2005 rejected claim 1 under 35 U.S.C. § 102(e)as being anticipated by USP 5,428,000 ("Hsieh"), rejected claim 2 under 35 U.S.C. § 103(a) as unpatentable over Hsieh in view of USP 5,202,593 ("Huang"), rejected claims 3, 8 and 16-17 under § 103(a) being unpatentable over Hsieh, in view of USP 4,922,445 ("Mizoue"), and rejected claims 9, 10 and 13-15 under § 103(a) as being unpatentable over Hsieh, in view of Mizoue and Huang. The office action also rejected claims 1-3, 8-10 and 13-17 under 35 U.S.C. § 102(b) as being anticipated by SPICE Library and Users Manual ("SPICE").

No claims have been amended, added or canceled. Hence, after entry of this amendment, claims 1-3, 8-10 and 13-17 will remain pending for examination.

II. The SPICE References

The office action rejected all pending claims under § 102(b) as being anticipated by SPICE. Those rejections are respectfully traversed.. Specifically, the Office provided two versions of a SPICE manual. The first version ("SPICE I") (entitled "SPICE 2G.1 User's Guide") is dated October 15, 1980. However, SPICE I does not disclose each element of any pending claim and is not relied upon in any specific rejection..

The second version (which the Office Action cites in rejecting claims 1-3, 8-10 and 13-17) is entitled "MicroSim PSpice & Basics Circuit Analysis Software User's Guide" ("SPICE II") and is dated June 1997. The present application, however, is a continuation of U.S. Application No. 08/299,395 (now USP 6,480,817) and therefore is entitled to the filing date of that application, which is September 1, 1994. SPICE II, therefore, is not prior art, and the applicants respectfully submit that the rejections of claims 1-3, 8-10 and 13-17 under § 102(b) should be withdrawn.

III. The Hsieh Reference

The office action also rejected claim 1 under § 102(e) as anticipated by Hsieh. Hsieh discloses an "Input/Output (I/O) Bidirectional Buffer for Interfacing I/O Ports of a Field Programmable Interconnection Device with Array Ports of a Cross-Point Switch." The buffer includes first and second unidirectional buffers connected for transmitting signals in opposite directions between first and second buses. (Abstract).

Hsieh, however, does not teach or suggest a system for modeling bi-directional signals of an electric circuit, as recited by claim 1. The simulation system of claim 1 is not a bidirectional buffer. Instead, it is a system for simulating (or modeling) signals in an electronic circuit. This is fundamentally different from an electronic circuit itself, which is what Hsieh discloses. (As the office action correctly notes in rejecting claim 10, "Hsieh does not teach simulating a bi-direction signal of a logic design.")

Moreover, the applicants respectfully submit that Hsieh, even if it could be considered a simulation system, fails to teach or suggest each element of claim 1. Merely by way of example, claim 1 recites "means for maintaining a first value representing an input component of the bi-directional signal; means for maintaining a second value representing an output component of the bi-directional signal; and means for generating a third value based upon at least the first value and second value." The office action presumes that one buffer (e.g., 100) acts as an input buffer while another (e.g., 102) acts as an output buffer.

The office action posits that the single-shot device (e.g., 104) might function as the means to generate a third value based upon at least the first value and the second value. The single-shot device 104, however, does not generate a third value, based on the first value and the second value. Rather, it merely determines whether buffer 100 should be driven low or high, depending on the desired direction of data flow. That is, the buffer 94 of Fig. 4 merely modifies the first value and/or the second value based on other inputs, rather than generating a third value. (See, e.g., c. 7, ll. 4-31).

Hence, Hsieh fails to teach or suggest the elements of claim 1, and claim 1 therefore is allowable over Hsieh. Claim 8, which is directed to a method of modeling a bi-directional signal of an electric circuit, recites elements similar to those of claim 1, and is

allowable for similar reasons, as is claim 16, which is directed to a method of operating an improved cell pad model, and which recites elements similar to those of claims 1 and 8. Claims 2, 3, 9, 10 and 17, each of which depend from either claim 1, claim 8, or claim 16, are allowable as being directed to allowable base claims and as reciting specific novel substitutes.

IV. The Huang Reference

As noted above and conceded by the office action, Hsieh fails to teach or suggest simulating a bi-directional signal. Huang, which is directed to a Bi-Directional Bus Repeater, likewise fails to teach either a method or system of simulating a bi-directional signal, and it therefore adds nothing to the disclosure of Hsieh in this regard.

V. The Mizoue Reference

The office action cites Mizoue (together with Hsieh and, in some cases, Huang) in rejecting claims 3, 8-10, and 13-17 under § 103(a). Mizoue is directed to a Logic Circuit Simulation Method, in which the output from a plurality of logic blocks 5 and 6 are provided as input (along with input data 3) to a logic simulator 1, which generates simulation output 4 and 9 (see Fig. 1 of Mizoue). Relevant to the present claims, Mizoue teaches only a method of simulating a simple electronic circuit and outputting the results to a computer file.

Mizoue, however, does not teach or suggest the elements of any pending claim, either by itself or in combination with Hsieh and Huang. In particular, Mizoue does not remedy the failings of Hsieh and Huang, discussed above.

Moreover, there is no motivation or suggestion to combine Mizoue with the teachings of Hsieh and/or Huang. Mizoue discloses a system for simulating a logic circuit, while Hsieh and Huang teach bi-directional circuits. There is no teaching or suggestion that Mizoue can model a bi-directional circuit, or even that the method of Mizoue might be modified to do so. Nor is there any teaching or suggestion in Hsieh or Huang that the circuits disclosed in those references might be modeled by a method such as that described in Mizoue. Rather, the office action engages in impermissible hindsight, effectively reasoning, based only on the disclosure of the present application, that Mizoue might be used to model a bi-directional circuit.

This reasoning is supported by nothing in the disclosure of Mizoue (or, for that matter, Hsieh or Huang). The office action posits that c. 6, ll. 36-44 of Mizoue "teaches a switch-level simulator that works for bi-directional switches." This statement cannot possibly be correct, because column 6 of Mizoue is only 21 lines long. Moreover, the applicants can find nothing in Mizoue that indicates that Mizoue might be able to model a bi-directional switch. Instead, Mizoue simply is configured to simulate the output from one or more logic blocks based on a series of inputs.

Further, there would be no reasonable expectation of success in the combination of Mizoue with Hsieh and/or Huang. Mizoue simply has no facility for dealing with a bi-directional signal. Hence, attempting to use the method of Mizoue to model a bi-directional signal, such as those generated in the circuits of Hsieh and Huang, would have no reasonable expectation of success.

MPEP § 2143 establishes three criteria for establishing a prima facie case of obviousness under § 103(a): "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." The rejections of claims 3, 8-10, and 13-17 meet none of these three criteria, and the applicants respectfully submit that rejections therefore should be withdrawn.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

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